## REMARKS

Claims 1-10 and 19-24 are all the claims pending in the application. Claims 11-18 have been withdrawn in response to a previously-filed Restriction Requirement, and are canceled, above. Claims 4-10, 22, and 23 stand objected to only as being dependent upon a rejected base claim, and would be allowable if rewritten in independent form to include all the limitations of the base claim and any intervening claims. Claims 4 and 22 have been rewritten in independent form to place claims 4-10, 22, and 23 in condition for immediate allowance.

Claims 1, 5, and 6 stand rejected upon informalities. Claims 1-3, 19-21, and 24 stand rejected on prior art grounds. In addition, the drawings and specification are objected to. Applicant respectfully traverse these objections/rejections based on the following discussion.

### I. Drawing and Specification Objections

With respect to the objections to the specification, the specification has been amended above, to overcome these objections. With respect to the objection to the drawings, Replacement Sheets are submitted herewith. More specifically, Figures 1A and 1B are designated "Prior Art". Further, with respect to the objection to Figure 2, paragraph 30 of the specification has been amended to correctly identify Receiver 261. In view of the foregoing, the Examiner is respectfully requested to withdraw the objections to Figures 1A, 1B, and 2.

Figs. 1C and 8 are objected to under 37 CFR 1.83 as failing to show all the details

claimed in claims 1 and 19. More specifically, the Office Action argues that the following items are not disclosed in the drawings and specification: 1) adjustable delay circuitry, 2) phase monitor, and 3) controller. In response, Applicant respectfully directs the reader's attention to the programmable or adjustable delay units 200-205 that are shown in Figure 2. As explained in paragraph 35, these adjustable delay units 200-205 are shown in greater detail in Figures 3A-4. Therefore, Applicant respectfully submits that the drawings and specification disclose the claimed adjustable delay circuitry. With respect to the phase monitor, Applicant directs the reader's attention to Figure 8 and paragraph 51 of the specification which illustrate the phase monitor 803. Again, Applicant submit that the drawings and specification disclose the claimed phase monitor. With respect to the controller, Applicant directs the reader's attention to Figure 1C and paragraph 29 of the specification which illustrate and discuss the controllers 250, 251. Thus, Applicant submits that the drawings and specification disclose the claimed controller. In view of the foregoing, the Examiner is respectfully requested to withdraw the objections to Figures 1C and 8.

The specification is objected to with respect to the description of Fig. 2. In response, paragraph 30 and 31 of the specification have been amended to consistently identify item 230 as the configuration word interface. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objection to the specification.

## II. The Prior Art Rejections

Claims 1-3 and 19-21 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kato et al., hereinafter "Kato" (5,394,490). Claim 24 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kato in view of Ernst et al., hereinafter "Ernst" (2002/0160558). Applicant respectfully traverses these rejections based on the following discussion.

### A. The Rejection Based on Kato

Applicant respectfully traverses this rejection because Kato does not teach or suggest "delay time set registers connected to said delay circuitry and said phase monitor, said delay time set registers adjusting said delay circuitry to compensate for said phase differences" as defined by independent claim 1 or "adjusting delay circuitry within said circuits to compensate for said phase differences using delay time set registers" as defined by independent claim 19. This is shown in Applicant's Figure 2, where the delay time set registers (DL registers 210-215) are connected to the adjustable delay circuitry 200-205. To the contrary, in Figure 11 of Kato a more expensive delay controller 1013 is connected to the programmable delay line 1012. The inventive structure/method produces cost saving and simplifies the structure thereby increasing yield and reliability by using simple registers in place of a more complex controller.

The field of the disclosure is a fast digital data transfer system (see line 1 of paragraph 4) therefore, the signals described in the disclosure include both data and clock signals. Also the

chip and signal carrier in the disclosure comprise a large printed circuit board (PCB), such as a computer mother board or back plane. The size of the PCB can be up to several tenths of inches or centimeters. A typical case can be two high speed micro processors or micro controller with multi bit (for example 64 bits) high speed data /clock bus connecting them, each bit being one signal channel.

Since the system mentioned in the disclosure is digital, the unit of the data transfer rate is Gbits /second or Gb/s (see line 1 of paragraph 8). One goal of the disclosure is to make good timing not only between data and clock in side of one data channel, but also among the multi channels (see paragraphs 4, 9, 10, 12, 13). This means that the reading edges of each clock of all channels occur at the time and around the middle of the data signals.

The signal connection and the carrier in the disclosure comprise printed circuit boards and metal transmission lines such as microstrip, stripline, etc. (see line 1 of paragraph 7). The disclosure includes a dynamic timing reference. Any timing adjustment must have a timing reference. In a conventional system, the timing reference is preset and cannot be used for the timing adjustments among multi channels. The timing reference in the disclosure is selected dynamically and on line (see line 14 of paragraph 13). Fig. 6(a) and Fig.6(b) show the circuits that can select the rising edge of longest delay data signal as the common time reference for the data and clocks for all channels (see paragraphs 42 and 43). In the disclosure, the programmable delay unit is not only used for the clock signal, but also for the data signal in each channel to reach a good timing among all channels (see line 4-5 of paragraph 30).

A slow serial communication data and clock is added between the controller and the

receiver in a high speed data transfer system to transfer the information of adjusting timing (see Fig. 1(c) and paragraph 31). The circuits of three programmable delay units are illustrated in Fig. Fig.3 (a), Fig.3 (b) and Fig.4. There are two steps of timing adjustments: step1- data-clock timing adjustment in each channel; and step 2 - timing adjustments among channels (see paragraph 33). Step 2 is divided into two sub steps: data to data (signal to signal) alignment; and data (signal) to clock alignment (see paragraphs 46 and 47). The timing is checked in the controller, and the final signal destination, then the adjustment information is sent to the receiver by the slow serial communication port (see Fig.6 (a) and Fig. 7). Therefore, the timing adjustment is superior to conventional structures and methods.

The circuits of the phase to voltage converter are illustrated in Fig.5. Advantages of using a phase to voltage converter over a phase comparator or phase detector includes that the output of the phase to voltage converter is a DC voltage whose magnitude is proportional to the input signal phase difference. Since this is a DC voltage, post processing is made very easy (for example, it can be digitalized by a simple analog to digital converter). To the contrary, the output of a phase comparator is still a phase which is the phase difference of the input signals, the output phase has higher frequency than the input signal, and the post processing of the phase is complicated (for example a controller must be used).

To the contrary, the structure of Kato is for clock signals only (see line 1 of Abstract). No timing between the data and clock signal and timing among data to data are described in Kato. Therefore, the field of Kato is entirely different field from that of the disclosure. The structure of Kato is a semiconductor flip-chip and a wring substrate and optical waveguide, that are inside of

an integrated circuit chip or an integrated chip package. The size of the substrate is in the millimeter range, much smaller than that in the disclosure. Also, in Kato nothing is related to multi channel data clock timing in printed circuit boards that can have the size of several tenths of an inch. Therefore, as a first point, the art field of Kato is different from that of the disclosure.

The goal of Kato is to make the clock signal without any phase deviation (see line 12 of Abstract). The timing adjustment of Kato is based on the information from the unit of distributor, not from the destinations (see Fig. 11). Thus, in Kato, the phase variations occur in the connections from the distributor and the destinations, and the phase delay variation inside of the destination cannot be adjusted. To the contrary, the claimed timing adjustment is based on the information in the final destination, the controller, so that the timing adjustment is more accurate. Therefore, the timing adjustment quality of the disclosure is better than that of Kato.

The timing reference of Kato is preset or fixed from the settings of the flip-flops (see Fig.11). This kind of timing reference has two disadvantages, it cannot adjust timing among channels and the delay unit cannot move the signal forward, but backward only. In such a system, when the reference timing signal is earlier than the clock signal, the delay unit in the clock signal chain fails to do the adjustment, or the delay unit has to set a very long delay time to the next cycle. It is well known that a long delay time will cause large jitter. This situation would likely occur in the system of Kato because the clock signal is transferred in optical units which can include a laser driver, laser diode, optical fiber, optical amplifier, photo diode, driver, band pass device and signal discriminator (see Fig. 12 and Fig. 13). Each stage contributes to the time delay. The reference signal from the same signal source goes through one stage of flip-flop

and electrical connections. The delay time is much shorter than the clock signal. In the present invention, the dynamic and on line reference selection guarantees that the signal with longest delay time will be the reference.

One example of the differences between the invention and Kato can be seen by comparing Fig.11 of Kato with Fig. 2 of the disclosure. As can be seen, the number of programmable units in each channel is different. One programmable unit 1012 is used in Kato, while multiple units 200-205 are used per channeling the disclosure. One advantage of multiple delay units is that the programmable delay can be used for both the clock and data signals. Also, a phase comparator 1011 is used in each channel of Kato, while a single phase voltage converter based timing adjustor is used in the inventive communication controller, not in each channel.

Further, a delay controller 1013 is used in Kato, while registers are used in the disclosure. More specifically, independent claim 1 defines "delay time set registers connected to said delay circuitry and said phase monitor, said delay time set registers adjusting said delay circuitry to compensate for said phase differences" and independent claim 19 defines "adjusting delay circuitry within said circuits to compensate for said phase differences using delay time set registers." A register is much simpler and cheaper than a controller.

The devices used in Kato are very expensive (such as laser, optical amplifier, etc.) while the devices used in the disclosure can be CMOS base gate and metal, which are very inexpensive. Thus, as shown above, the field, the goals, and the applications of Kato are different from those of the disclosure. In the circuit and the method embodiments, the claimed invention produces better performance, has wider applications, and is lower in cost than Kato.

Thus, as shown above, Kato does not teach or suggest "delay time set registers connected to said delay circuitry and said phase monitor, said delay time set registers adjusting said delay circuitry to compensate for said phase differences" as defined by independent claim 1 or "adjusting delay circuitry within said circuits to compensate for said phase differences using delay time set registers" as defined by independent claim 19. Thus, Applicant respectfully submits that independent claims 1 and 19 are not disclosed by Katom and are therefore not anticipated by Kato. Further, dependent claims 2, 3, 20, and 21 are similarly not anticipated by Kato, not only because they depended from a patentable independent claim, but also because of the additional features of the invention they define. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw his rejection.

**B. The Rejection Based on Kato in view of Ernst**

Applicant respectfully traverses this rejection because even if Kato were combined with Ernst, the proposed combination does not teach or "adjusting delay circuitry within said circuits to compensate for said phase differences using delay time set registers" as defined by independent claim 19.

The field of the Ernst is DRAM module testing (see Line 3 of Abstract) which is entirely different from that of the disclosure. The goal of Ernst is reading and checking the time position of a data response read out from a memory module to be tested (see line 1 to 2 of Abstract). The goal is not related to anything of data to clock timing adjustment or data to data timing

alignment. Therefore the goal of the application is entirely different from that of the disclosure. Therefore, Applicant initially submits that a prima facie case of obviousness has not been set forth because one ordinarily skilled in the art would not have made the proposed combination of references.

Further, Ernst does not teach or suggest the utilization of delay time set registers as in the claimed invention (and the Office Action does not propose that Ernst provides such teaching). Therefore, no combination of Kato and Ernst would teach or suggest the invention defined by independent claim 19. Applicant respectfully submits that independent claim 19 is patentable over the proposed combination of Kato and Ernst. Further, dependent claim 24 is also patentable, not only by virtue of the dependency from independent claim 19, but also by virtue of the features dependent claim 24 defines. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

## III. Formal Matters and Conclusion

The claims are objected to because of various informalities. The claims have been amended as suggested in the Office Action in order to overcome these objections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw these objections. In addition, the use of the phrase "adapted to" is objected to as not being a positive limitation. In response thereto, the offending language has been removed from the claims. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objections to

the claims.

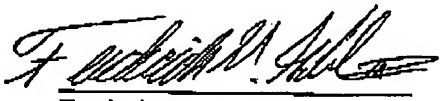
Applicant submit that claims1-10 and 19-24, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: 6-21-05



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